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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/539,839      | 03/31/2000  | Ariel Berkovits      | 2207/6856           | 9593             |

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EXAMINER

PEUGH, BRIAN R

| ART UNIT | PAPER NUMBER |
|----------|--------------|
| 2186     |              |

DATE MAILED: 05/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

|                 |                |              |                  |
|-----------------|----------------|--------------|------------------|
| Application No. | 09/539,839     | Applicant(s) | BERKOVITS, ARIEL |
| Examiner        | Brian R. Peugh | Art Unit     | 2186             |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

1) Responsive to communication(s) filed on 31 March 2000.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

4) Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-30 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Disposition of Claims

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_ .  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)  
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ . 6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Objections***

1. Claim 6 is objected to because of the following informalities: Please replace "in" with --is--. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
3. Claims 4, 12, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
4. Claims 4, 12, and 20 recites the limitation "the other line" in line 2. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 9-13, 17-21, and 25-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Csoppenszky (US# 5,802,568).

Regarding claims 1, 9, 17, 25, 26, and 30, Csoppenszky teaches pseudo-LRU caching system including an invalidation scheme in associative caches. One of ordinary skill in the art would know that there are many reasons for invalidating a cache line, such as in Csoppenszky's example (column 5, lines 12-24). For instance, the phrase "unless invalidated by the processor core" indicates that the processor can invalidate cache entries. Another invalidation instance would occur from other operations such as a cache miss in one of many processors on a bus, the one processor sending a command for the other processors to relinquish ownership of the cache line and invalidate all copies of the cache line in their cache memories, which is also known to those of ordinary skill in the art.

Regarding claims 2, 9 (cont.), 10, 18, 27, and 30, by invalidating a cache line, the cache line's importance has been reduced to the point of being replaced before all other valid cache lines (column 1, lines 58-60; abs.).

Regarding claims 3, 11, 19, and 28, invalidated cache lines are replaced before other valid cache lines which adhere to the LRU scheme (abs., lines 3-5; column 1, lines 58-60).

Regarding claims 4, 12, and 20, the replacement policy as noted above is an LRU policy. Since any item in the cache could be marked with an invalidation flag at any time, it is possible that the most least-recently used item may not be the item selected for invalidation.

Regarding claims 5, 13, 21, and 29, when an item has been invalidated, the item will be replaced prior to the least-recently-used item according to the LRU policy, thus altering the policy by not replacing what would have been the next cache item to be replaced but rather that of the invalidated cache item.

Regarding claims 8, 16, and 24, the invalidation of a cache line corresponds to

Regarding claim 17 (cont.), one of ordinary skill in the art would appreciate that for any type of replacement system to occur, here a pseudo-LRU with invalidation replacement scheme, the conditions and operational instructions necessary for the replacement system to work must be stored within a data storage system within the computing system. Since the replacement system of Csoppenszky includes the above-mentioned scheme, the replacement system must inherently store the means for which to do so in any number of locations, such as on the processor itself or within an external data storage device.

Regarding claim 25 (cont.), although not explicitly stated, for cache operations to occur on cache lines with corresponding (valid) bits, some form of cache control logic must be present and therefore would be inherent to the teaching of Csoppenszky.

#### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 6, 7, 14, 15, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Csoppenszky (US# 5,802,568) and Funk et al. (US# 6,314,561).

9. The difference between the claimed subject matter and that of Csoppenszky, disclosed *supra*, is that the claims recite that the replacement instruction is generated by a compiler or is part of an application kernel. Regarding claims 7, 15, and 23, Funk et al. teaches a data cache management mechanism that is created by an optimizing compiler. The compiler places non-blocking preload instructions into the instruction stream of the computer system so as to minimize both the frequency and detrimental effect of cache misses (column 3, lines 17-22). Thus, the compiler hopes to minimize cache misses by loading data from the main memory into the cache. This directly relates to the cache loading and replacement scheme of Csoppenszky. The creation of the data cache management mechanism relates to the claimed material of claims 6, 14, and 22, in that a kernel is a core processing mechanism used within a computer system. The optimization compiler of Csoppenszky sends commands for optimizing the caching system as well as controlling the data cache management mechanism, such that parts of the mechanism are present in all mechanism that were compiled by the optimization compiler (column 6, line 66 – column 7, line 11). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Csoppenszky and Funk et al. before him at the time the invention was made to modify the caching system of Csoppenszky to include the optimization compiler/data cache management

mechanism of Funk et al., because then instruction could be pre-loaded into the instruction stream in order to curb the frequency of cache misses, as taught by Funk et al.

10. Claims 8, 16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Csoppenszky (US# 5,802,568) and Worley, Jr. et al.

11. The difference between the claimed subject matter and that of Csoppenszky, disclosed *supra*, is that the claims recite that an instruction for designating replacement is an extension of a memory access instruction. Worley, Jr. et al. teaches a caching system with a corresponding flush data cache instruction. The instruction sets the cache line's valid bit to "invalid" if the data hits the cache. The cache line is then written back to main memory if the cache line's dirty bit is set (column 4, lines 36-40). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Csoppenszky and Worley, Jr. et al. before him at the time the invention was made to modify the caching and invalidation scheme of Csoppenszky to include the flush data cache instruction of Worley, Jr. et al., because then a system for writing back altered data to the main memory would be in place that would negate the loss of potentially important information, as taught by Worley, Jr. et al.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art teaches related LRU and pseudo-LRU replacement schemes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Friday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim, can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

*BRP*  
MMK/BRP  
May 3, 2002

  
MATTHEW M. KIM  
SUPERVISORY PATENT EXAMINER  
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